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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,948	RHOADES ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 09/30/02.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-58 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-58 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09/30/02 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☑ All b)☐ Some * c)☐ None of:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 09/30/02 (Modified 1449)
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-58 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11,17-22, 32, 34 , 38, 39, 40, 44-46, 50,51,52,56,57 are rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Childers et al. (5,986,913).

2. As to claims 1-5,7-9, 10, 11, 19, 20,32, 34,52, Childers disclosed at least :

a) an input and output device (or system) for receiving data packets (see fig.1 [data input]);

A plurality of processing elements to receive the data input (see fig.1 [10], see [10] as a plurality of SIMD processing elements in col.3, lines 34-40, see fig.2 for the structure of each PE);

Wherein the input device was operable to distribute data packets in whole or in part (e.g. 1 to 1024 words) to the processing element depending the bandwidth [40 bit wide] of the processing elements (see col.4, lines 15-23).

3. As to claim 6, Childers disclosed that his processing elements process the input data with delay time to complete the pipeline (see col.3, lines 60-67, col.4, lines 1-1-6), therefore, not all the processing element receive data at a given time.

AS to claims 17,18, 38, 39, 56,57, Childers taught a plurality of processing elements operable to transfer data in and out of the processing elements (see fig.1 [10], see [10] as a plurality of SIMD processing elements in col.3, lines 34-40, see fig.2 for the structure of each PE), and capable of processing a single packet (e.g. see 1 to 1024 words).

4. As to claims 21,40, 44, 45, Childers was also directed to s single integrated circuit (see integrated circuit in fig.1 [10]).

5. As to claim 22,46, 50,51, Childers was also included in plurality of integrated circuits (in col.1, lines 39-40, see also the variation of the processing elements in col.3, lines 20-23).

6.

7. Claims 12,13 , 35, 41, 47,53 are rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Gove et al. (5,371,896).

8. As to claims 12,13,35, 41,53, Gove discloses SIMD including a plurality of processing elements [PE 300] operable to receive data and included a stand-by of operation (see the wait signal in col.56, lines 48-52).As to claim 47, Gove also included plurality of integrated circuits (see fig.1).

9. Claims 23-31, 58 are rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Horst (5,404,550).

10. As to claims 23,25, 58 Horst disclosed a SIMD system including e plurality of processing elements (see fig.6, col.1, lines 7-22 for background, see also col.2, lines 61-66 for the processing elements) operable to transfer data packet of different size respective to the processing elements (see variable packet size in col.5, lines 14-18).

11. As to claim 24, Horst also included different addresses because the (e.g. see the received packet in different entries of the queue in col.11, lines 20-50, see also fig.15).

12. As to claims 26-28, Horst also directed to a batch of packets (see plurality of packets queues in col.11, lines 7-19).

13. As to claims 29-31, Horst also included transfer of the batches depending on the processing speed (see the readout of the waiting packet in col.11, lines 8-68, col.12, lines 1-9).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14,15 ,16,33,36,37, 42,43, 48,49, 54,55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (5,872,993) in view of Childers et al. (5,986,913).

14. As to claims 14,15, 36,37, 54, 55, Brown disclosed a data processing system (see fig.3) including at least :

a) hardware accelerator [HW ACC] operable to receive processing requests from processing elements and return result to the processing elements (see the read/write requests tot eh hardware accelerator in col.25, lines 5-40, col.27, lines 50-67, col.28, lines 1-39, see how DSP communicated with HW ACC in col.7, lines 50-62, see the MCU and DFP as the functional operations with the DSP in col.7, lines 3-47 for background);

b) input/output system for transferring requests form the processing elements (see the DSP 300 and second DSP 360, col.6, lines 45-49) to the e hardware accelerator (e.g. see the DFP as an interface control in col.25, lines 5-40, col.27, lines 50-67, col.28, lines 1-39) ;

c) wherein the processing elements are operable to process the results when all such results were returned (see the data input and output from HW ACC in col.25, lines 5-40, col.27, lines 50-67, col.28, lines 1-67, col.29, lines 1-67, col.30, lines 1-21).

15. Brown did not specifically show his processing elements (the DSPs) were single instruction and multiple data as claimed. However Childers disclosed a system including single instruction multiple data (e.g. see col.3, lines 34-40). It would have been obvious to one of ordinary skill in the art to use Childers in Brown for including the single instruction multiple data as claimed because the use of Childers could provide the processing capability of Brown to integrate a specific type of processing mode , such as the single instruction multiple data into the digital system of Brown, thereby, providing the ability to accept additional processing structure, and therefore, increasing the adaptability of the system, and it could be readily achieved by predefining

the single instruction and multiple data format of Childers with modified control parameters (e.g. the processing type and the mode switch single) into Brown so that the single instruction and multiple data format of Childers could be recognized by Brown in order to provide the enhanced processing capability, and for the above reasons , provided a motivation.

16. As to the order of the requests , see the request queuing in col.30, lines 12-21).

17. As to claims 16, 33, Brown also included a second hardware accelerator unit (e.g. see fig.3 [HW ACC 2).

18. As to claims 42,43, Brown was also directed to integrated circuit because it was an embedded DSP system (e.g. see col.10-25).

19. As to claims 48,49, Childers also included plurality of integrated circuits (see col.1, lines 39-40).

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Maher (6,301,603) is cited for the teaching of the plyrality of hardware accelerators (see fig.2);

b) Eilenberger et al. (4,922,487) is cited for the background teaching of the distribution of the plurality of packets (e.g. see 2, lines 21-40).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or

the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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